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AMENDMENTS TO THE SPECIFICATION

KINDLY AMEND THE SPECIFICATION AS FOLLOWS:

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Title: PLL/DLL Dual Loop Data Synchronization Utilizing a Granular FIFO Fill Level Indicator

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Cross Reference to Related Applications

This application includes subject matter that is related to and claims priority from U.S. Provisional Patent Application Serial No. 60/257,187, filed December 20, 2000 and entitled "Granular FIFO Fill Level Indicator for Multi-Period Asynchronous Data Phase Detection." This application further includes subject matter related to U.S. Patent Application No. 10/029,956, ~~XX/XXX,XXX,~~ filed on even date herewith, and entitled "PLL/DLL Dual Loop Data Synchronization."

Field of Invention

The present invention relates generally to a system and method for data synchronization and, in particular, to an improved phase locked loop/delayed lock loop (PLL/DLL) "dual loop" approach to data synchronization. More particularly, the present invention relates to a system and method for dual loop data synchronization using a granular FIFO fill level indicator.

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Further, traditional first-in first-out (FIFO) ~~FIFO~~ indicators or flags tend to allow or enable phase detectors to exhibit non-linear behavior, i.e., non-linear transfer functions, such as exhibited in non-linear "bang-bang" phase detectors.

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Page 12 paragraph [0041]

Referring now to Figure 7, an exemplary ~~a exemplary~~ block diagram of the retimer of Figure 6 is illustrated. Retimer 700 includes a dual loop serializer, comprising PLL 702 and DLL 704, and a DCDR, comprising DLL 703 and PLL 702. As previously discussed, in accordance with an exemplary embodiment of the invention, a single analog PLL 702 is used which includes a phase shifter. Analog PLL 702 provides a reference frequency multiplication or, creates a serial clock that is close to a multiple of the target frequency. Similar to PLL 502 of serializer 500, PLL 702 includes a PFD 706, a loop filter 711, a VCO 705, and a phase shifter 716.

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Page 16 paragraph [0050]

Figure 8 illustrates an exemplary block diagram of a granular FIFO fill level indicator system 800. FIFO fill level indicator system 800 is configured to facilitate the obtaining of a linear phase detector transfer function, which is highly desirable. Exemplary granular system 800 includes a write counter 802, a plurality of FIFO registers 804, a read counter 806, and a comparison module 808. Comparison module 808 can comprise various devices and components for performing comparing functions, such as subtraction. In this particular embodiment, granular system 800 uses comparison module 808 to determine a difference between a state in write counter 802 and a state in read counter 806. The difference is output from comparison module 808, which performs the difference function, and represents the fill level of FIFO registers 804. There may exist some difficulty in a direct implementation of fill level indicator system 800 because counters 802, 806 ~~804~~ are generally asynchronous. In other

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words, the write clock and the read clock are not synchronized so the inputs received from counters 802 and 806 are generally not equally timed. Accordingly, the techniques to follow describe various embodiments for implementing a FIFO fill level indicator system 800 for data synchronization having asynchronous read and write clocks.

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Page 17 paragraph [0054]

In accordance with another exemplary embodiment, with reference to Figure 11, an exemplary multi-phase detector based FIFO fill level indicator system 1100 for sampling the high speed write and read counters is shown. Similar to system 800, multi-phase detector system 1100 includes a write counter 1102, a plurality of FIFO registers 1104, a read counter 1106, and a comparison module 1108. In this particular embodiment, comparison module 1108 includes a plurality of phase detectors, e.g., three phase detectors, 1112-1114, and a binary decoder 1115. In this particular embodiment, multiple phases of write counter 1102 are sampled with read counter 1106. Multi-phase system 1100 is configured to provide additional granularity by including multiple phase detectors (e.g., 1112-1114) and sampling a greater number of phases from write counter 1102. In this manner, phase detector 1112 ~~748~~ may be represented as one of the clocked phases of read counter 1106 with one of the data inputs (phases) of write counter 1102. It should be noted that while three phase detectors 1112-1114 are illustrated, fewer or more phase detectors could also be implemented in other embodiments.

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